Dalhousie University Faculty of Computer Science
Introduction to Systems
Assignment 1 CSCI 1120 Due: 29 Sept 2022

Notes: *(i)* Please explain all your answers. An answer with no explanation/computations will not receive any credit. *(ii)* You may discuss the problems with your classmates, but work on your own. *(iii)* Getting answers of *homework aid services*/the internet *etc* is an academic integrity offence. *(iv)* You should start on the assignment. I will set up a submission box a bit later. I suggest you start each part on a new sheet of paper

(1) **[4+4]**
   (a) Determine the base b, given that $124_b = 103_{10}$.
   (b) If the solutions to the quadratic: $x^2 - 14x + 43 = 0$ are $x_1 = 7$ & $x_2 = 5$ (in decimal), what is the base of numbers in the quadratic equation?

(2) **[3+1]**
   (a) Show that the NOR gate is *complete*.

   (b) The **dual** of a Boolean function is obtained when $+ \longleftrightarrow \cdot$ and $0 \longleftrightarrow 1$. Identify the gate that is the dual of the NOR gate.

(3) **[2+2+4]** In class, we examined the two input Xor gate and took a look at its truth table.
   (a) Construct the truth table for the 3-input Xor gate (The truth-table **must** have the same form and ordering of rows as in the class notes).
   (b) Obtain the Boolean Function for representing the 3-input Xor gate is the sum-of-products (sum of minterms) form.
   (c) Now, suppose you want to transmit a 3-bit message $X\ Y\ Z$ plus an additional **parity bit** W. The parity bit W is generated such that it makes the number of '1' bits in the sent message $X\ Y\ Z\ W$ **even**. For example, if $X = 1\ Y = 0\ Z = 0$ then the **parity** bit $W = 1$ and the sent message is 1 0 0 1.
   Construct a circuit that outputs the parity bit W. Give the circuit diagram, with an explanation, of the (even) parity generator (*hint: examine 2.(a)*).

...contd →

[2 + 2 + 2 + 4]

(a) Find the canonical sum-of-products form of F given in the truth table below
(b) Find the negation of the expression for F you obtained above.
(c) Draw the logic circuit for the expression in (a) (using the basic gates AND OR, NOT).
(d) Use properties of Boolean algebra to reduce the expression to a network that requires only two logic gates.

X	Y	Z	F(X,Y,Z)
1	1	1	0
1	1	0	1
1	0	1	0
1	0	0	1
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0