

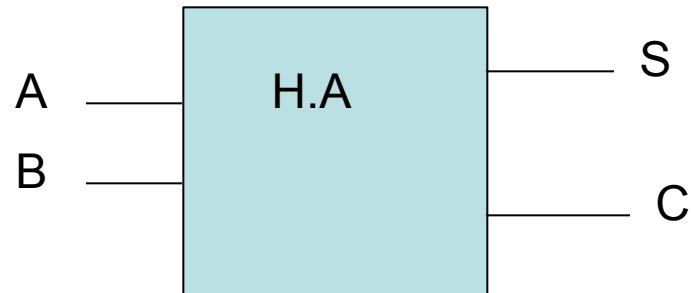
Combinatorial Circuits III

The Half Adder, the Full Adder,
the DeMux, the Encoder

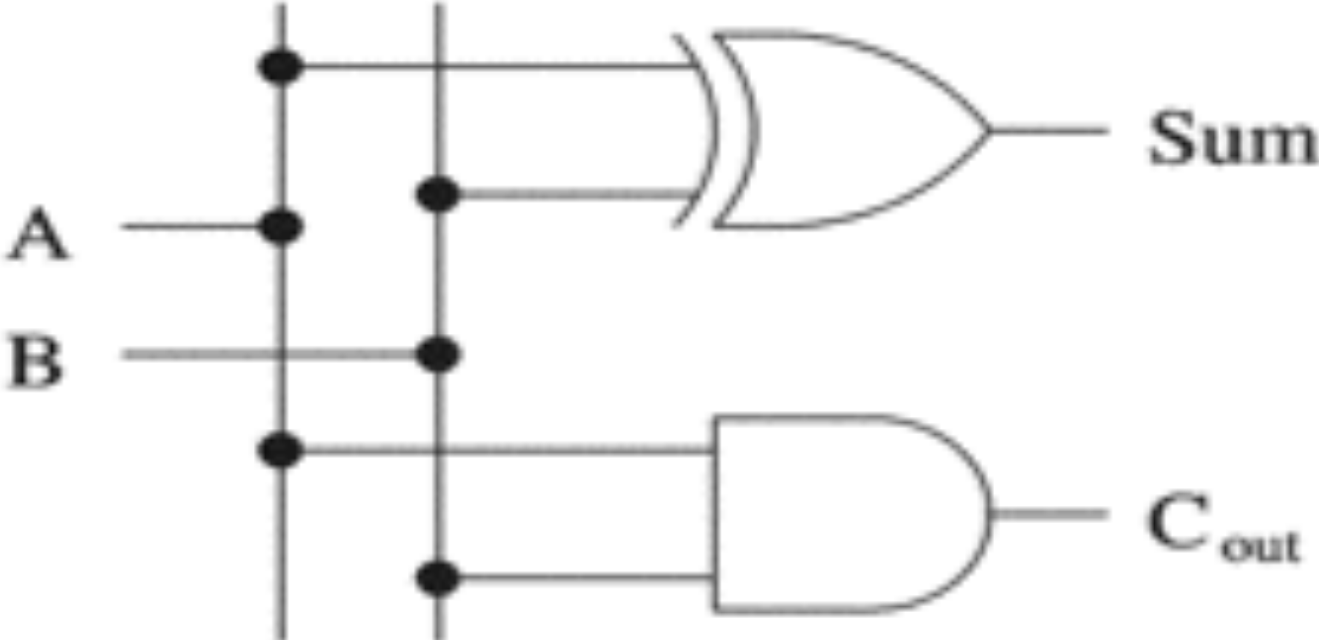
How do you add 2 bits?

A	B		S	C	
0	0		0	0	S =
0	1		1	0	
1	0		1	0	C =
1	1		0	1	

Why ``Half''?



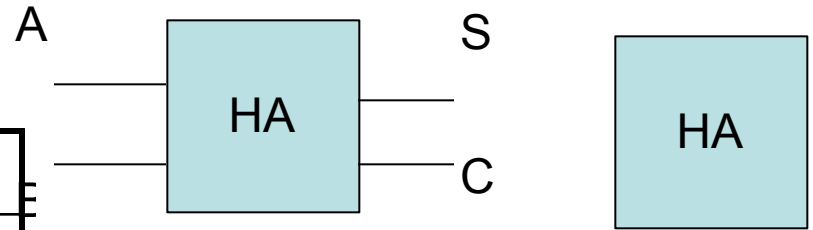
The Half Adder



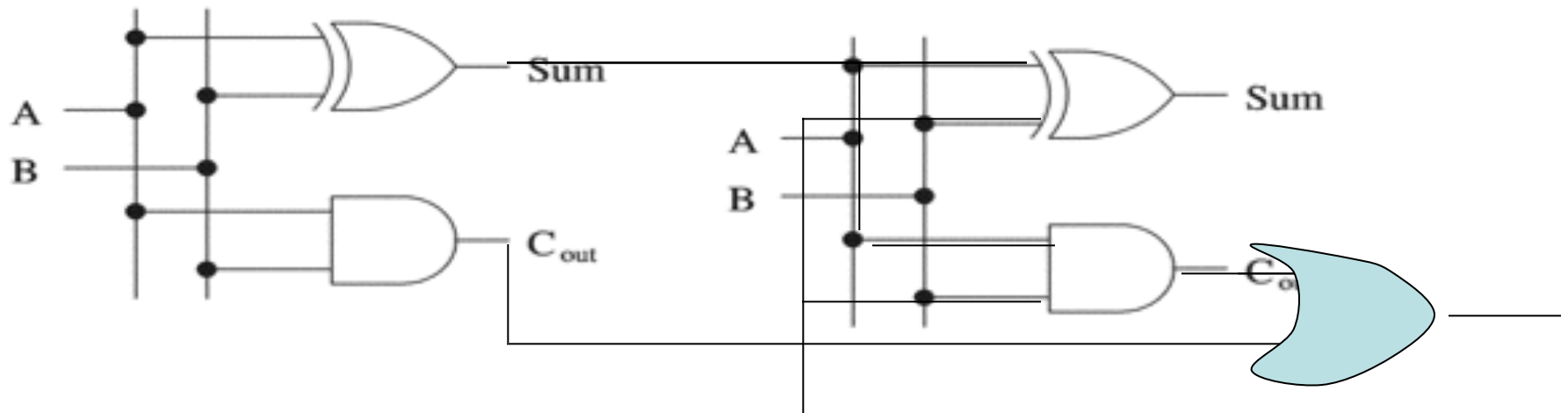
The Full Adder

- Truth table
- Sum = $A \oplus B \oplus C_{in}$
- $C_{out} = (A \cdot B) + (A \oplus B) \cdot C_{in}$

C _{in}	A	B	S	C _{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



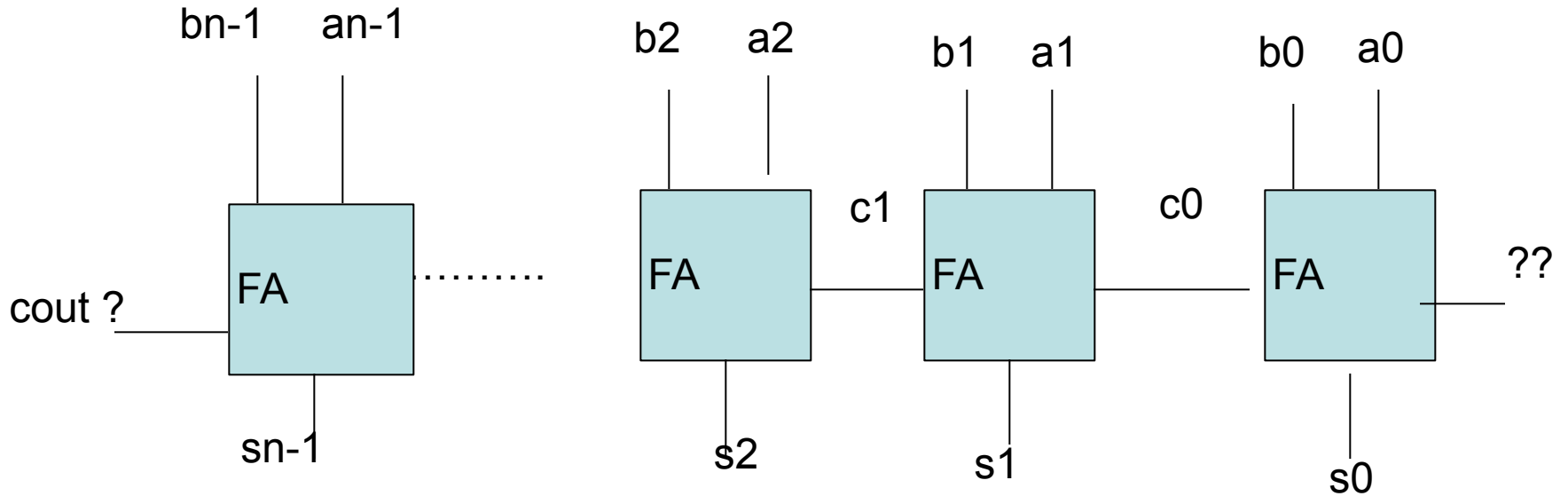
Full Adder



The n-bit Ripple Carry Adder

$a = a_{n-1} \dots a_2 a_1 a_0$

$+b = b_{n-1} \dots b_2 b_1 b_0$



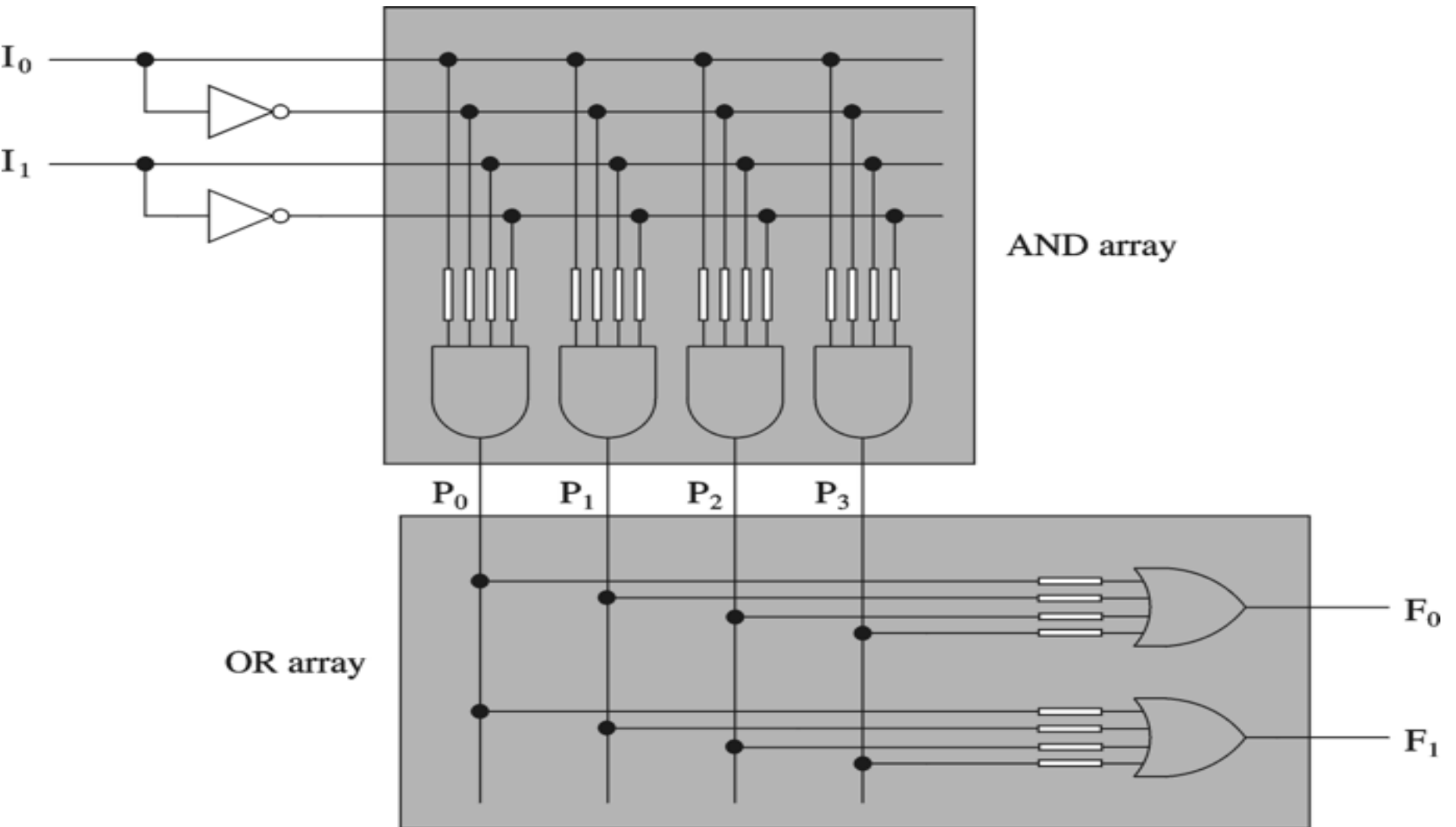
Ripple-Carry Adders (contd.)

- Ripple-carry adders can be slow
 - Delay proportional to number of bits added
- Carry lookahead adders
 - Eliminate the delay of ripple-carry adders -
 - Impl. carry in 2 parts: $G_i = A_i \cdot B_i$ & $P_i = A_i \text{ xor } B_i$
 - then $C_{i+1} = G_i + P_i \cdot C_i$ etc.
 - Carry-ins are generated independently
 - $C_0 = A_0 B_0$
 - $C_1 = A_0 B_0 A_1 + A_0 B_0 B_1 + A_1 B_1$
 -
 - Requires complex circuits
 - Usually, a combination carry lookahead and ripple-carry techniques are used

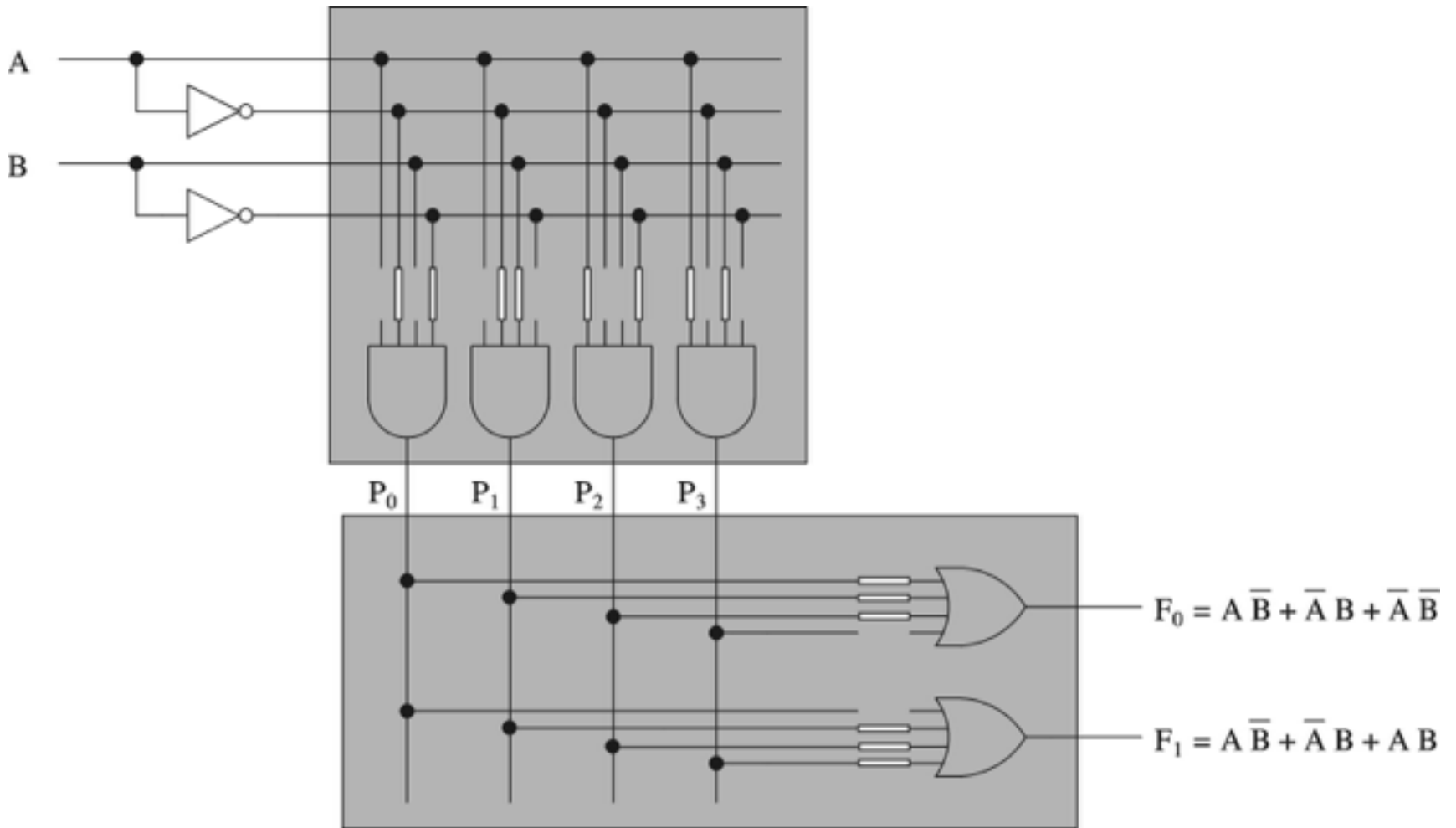
Practical Devices: Programmable Logic Arrays

- PLAs (also fPGA: field P Gate A)
 - Implement sum-of-product expressions
 - No need to simplify the logical expressions
 - Take N inputs and produce M outputs
 - Each input represents a logical variable
 - Each output represents a logical function output
 - Internally uses
 - An AND array
 - Each AND gate receives $2N$ inputs
 - » N inputs and their complements
 - An OR array

A 2 i/p 2 o/p PLA



Implementation of Boolean Functions using PLAs



Encoder/ Priority encoder

- A 2^n to n device that delivers the binary index of a bit pattern.
- Trouble with straight encoder.
- Hence:
- The MSB has highest priority etc.
- Used when multiple devices use the same resource. Each device is granted a priority that is used to resolve any conflicts.
- (circuit in class)

Table for a priority encoder

x_3	x_2	x_1	x_0	y_1	y_0
1	x	x	x	1	1
0	1	x	x	1	0
0	0	1	x	0	1
0	0	0	x	0	0