

Useful Digital Circuits

Combinatorial Circuits II

Derivation of logical expressions from truth tables

SOP (Sum Of Products) form:

- >Write an AND term for each input that produces a 1 output
Write the variable if its value is 1; complement otherwise
- >OR the AND terms to get the final expression

A	B	C	F	Minterms
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0	0	0	0	
---	---	---	---	--

0	0	1	0	
---	---	---	---	--

0	1	0	0	
---	---	---	---	--

0	1	1	1	--> $\overline{A}BC$
---	---	---	---	----------------------

1	0	0	0	
---	---	---	---	--

1	0	1	1	--> $A\overline{B}C$
---	---	---	---	----------------------

1	1	0	1	--> $AB\overline{C}$
---	---	---	---	----------------------

1	1	1	1	--> ABC
---	---	---	---	-----------

Sum of Minterms

$$F = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$

The POS form

The Product of Sums form is the **dual** of the **SOP** form.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Maxterms

$$(A+B+C)$$

$$(A+B+\bar{C})$$

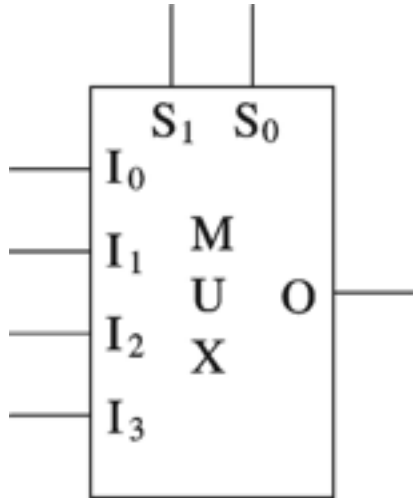
$$(A + \bar{B} + \bar{C})$$

— — —

$$(\bar{A} + B + C)$$

The Multiplexer

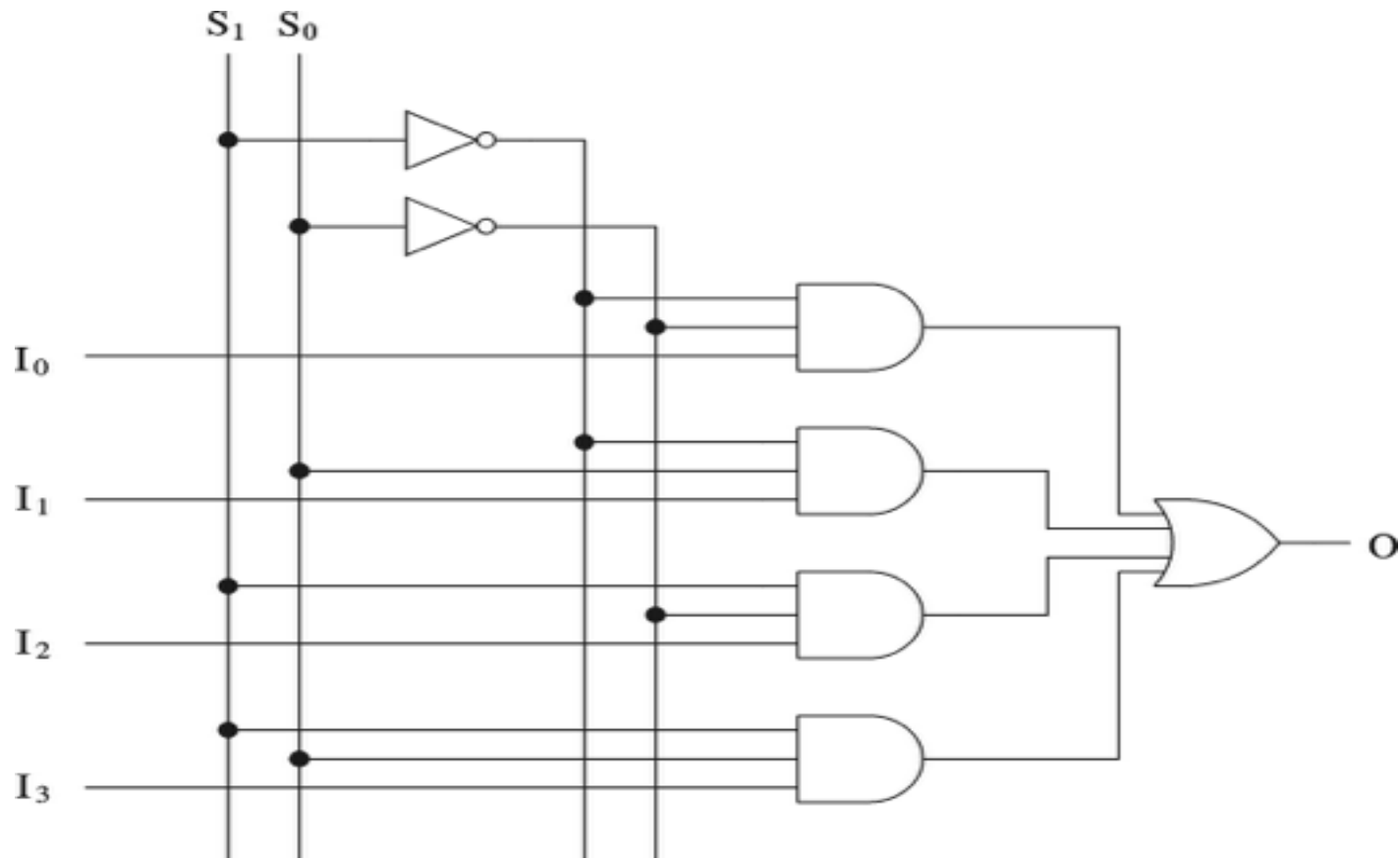
- Multiplexer
 - 2^n data inputs
 - n selection inputs
 - a single output



S_1	S_0	O
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

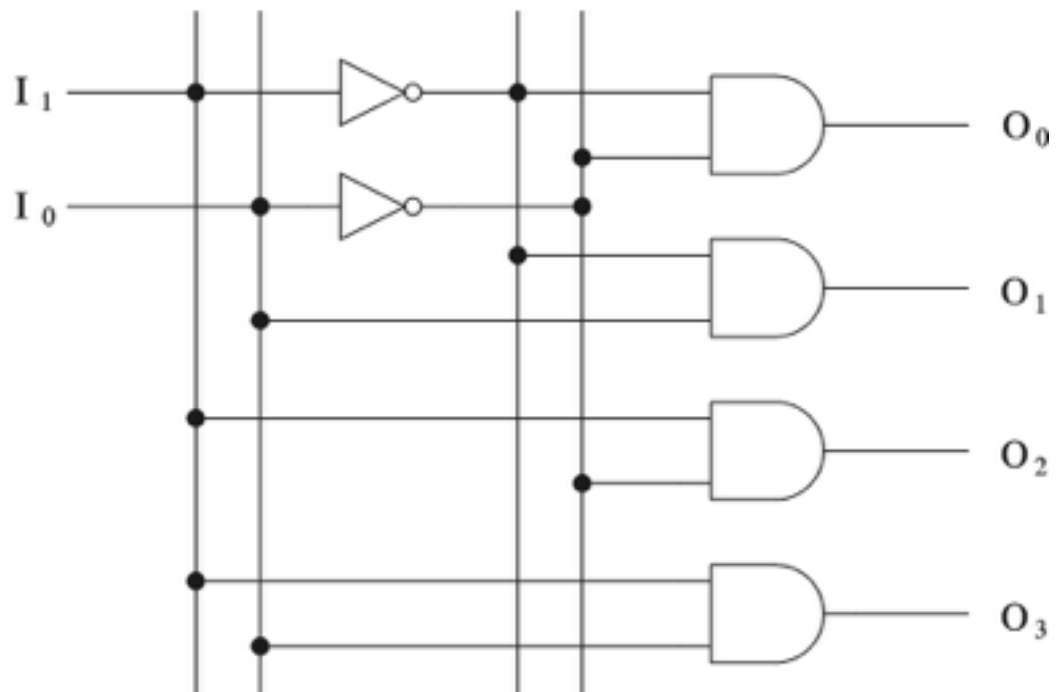
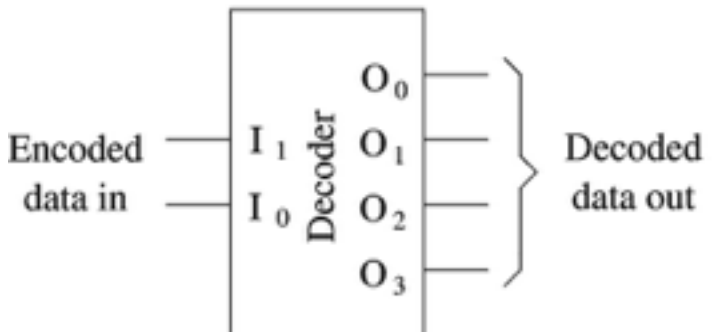
- Selection input determines the input that should be connected to the output

4 to 1 Mux Implementation



A decoder is a circuit that converts binary information from the n coded inputs to a maximum of 2^n unique o/p.

I_1	I_0	O_3	O_2	O_1	O_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0



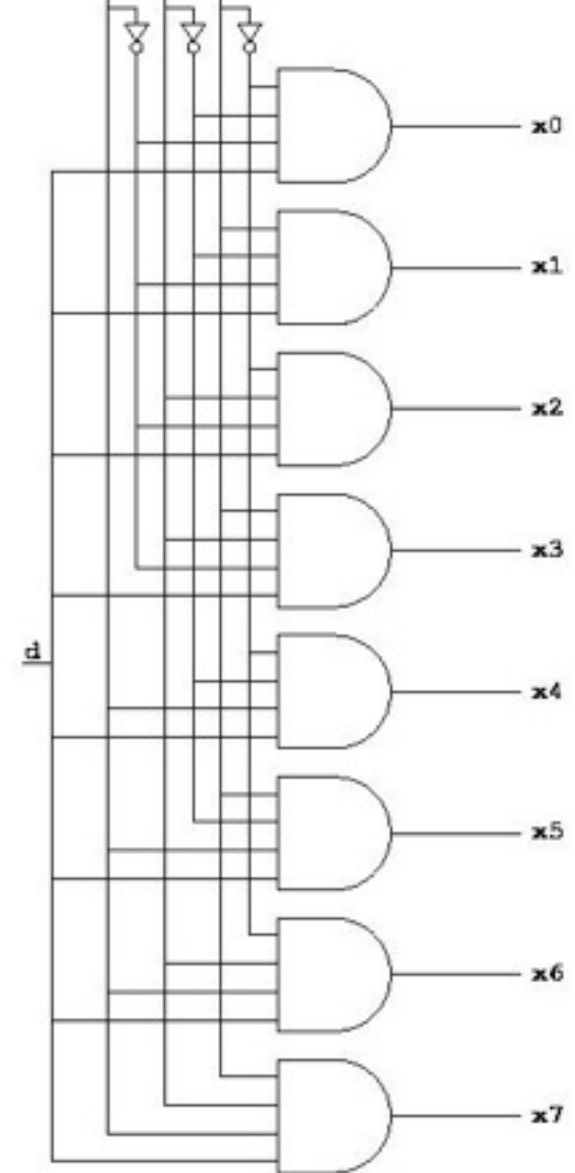
The Demux

- The inverse of the MUX; it has:

2^n outputs, 1 input and n selectors
(addressing) terminals

a2	a1	a0	d	x7	x6	x5	x4	x3	x2	x1	x0
0	0	0	c	0	0	0	0	0	0	0	c
0	0	1	c	0	0	0	0	0	0	c	0
0	1	0	c	0	0	0	0	0	c	0	0
0	1	1	c	0	0	0	0	c	0	0	0
1	0	0	c	0	0	0	c	0	0	0	0
1	0	1	c	0	0	c	0	0	0	0	0
1	1	0	c	0	c	0	0	0	0	0	0
1	1	1	c	c	0	0	0	0	0	0	0

Used to send data from a single source to one of a number of destinations. Is also a universal gate.

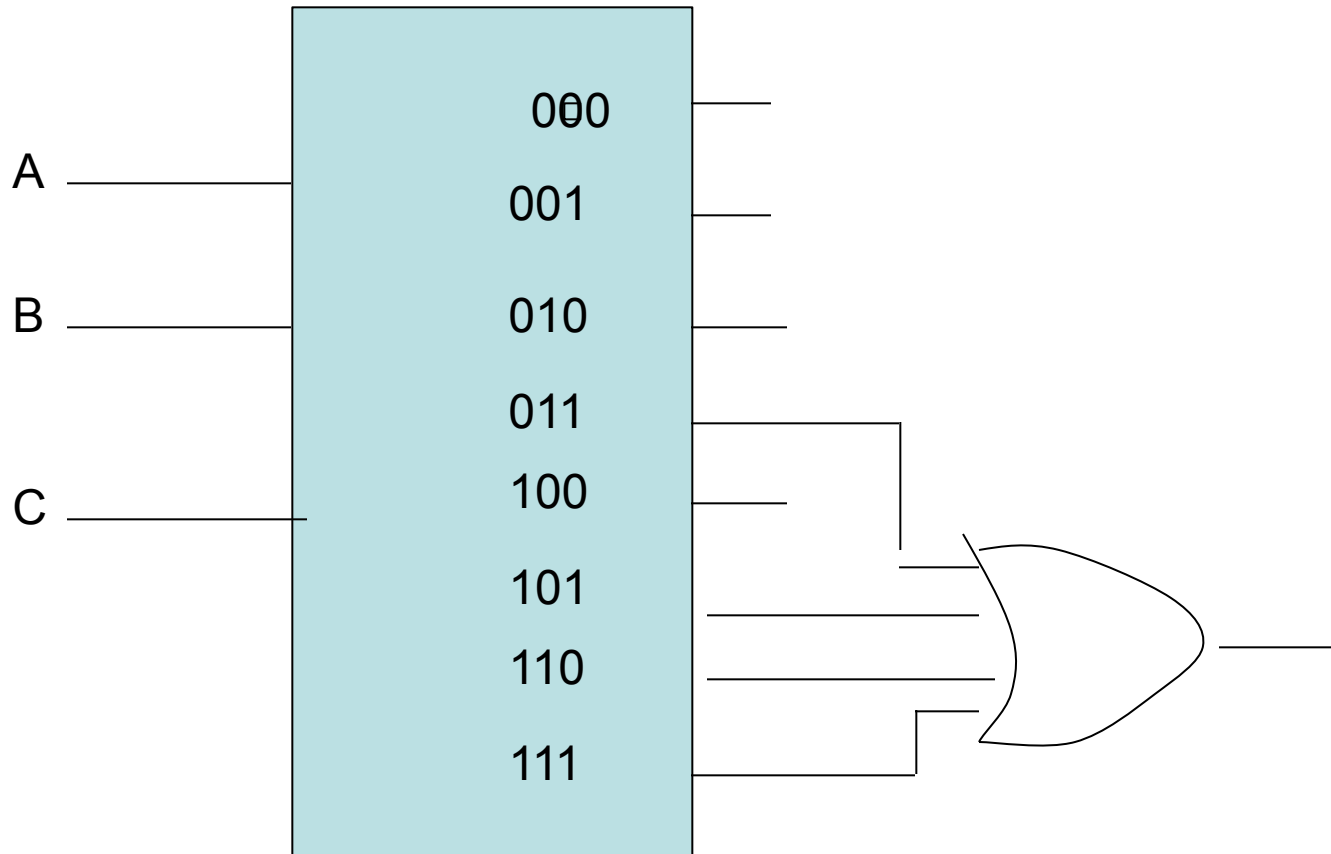


Decoder (contd.)

- Notice, that each o/p of the decoder is a minterm:
- $O_0 = \overline{I_2 I_1}$ $O_1 = \overline{I_2} I_1$ $O_2 = I_2 \overline{I_1}$ & $O_3 = I_2 I_1$
- Hence ANY B. Func. (which as we saw before, can be expressed as a sum of minterms) can be implemented with an (appropriate) decoder and OR gates.

Example:

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



Implementing Combinatorial Circuits with a Mux

- Examine the logic circuit of a MUX and compare it to the decoder - the MUX is essentially a decoder with an OR gate putting together all the o/p's
- The minterms of the function are generated by the selector bits and selected by the I/p bits:
- There is a method for impl. an n-variable B. Func. with a MUX with (n-1) selector inputs: (once again the majority func)

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

----- Connect the first (n-1 = 2) variables to Selector I/p

0 0 0 0

The remaining var. is used for the data I/ps

0 0 1 0

which will be C, \bar{C} , 1 or 0.

----- Here when AB = 00, F = 0, so apply 0 to I/p 0

0 1 0 0

when AB = 01, F = C so apply C to I/p 1

0 1 1 1

when AB = 10, F = C so apply C to I/p 2

----- when AB = 11, F = 1, so apply 1 to I/p 3

1 0 0 0

1 0 1 1

1 1 0 1

1 1 1 1

